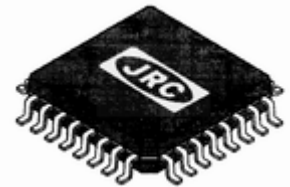# 3.1ch Outputs Digital Signal Processor

■ General Description

The NJU26105 is a high performance 24-bit digital signal processor.
The NJU26105 provides 'eala' 3D Surround function, 'eala BASS' Dynamic Bass Boost function, 5band-PEQ, AGC, and Tone Control. These kinds of sound functions are suitable for TV, mini-component, CD radio-cassette, speakers system and other audio products.

■Package

NJU26105FR1

■ FEATURES

- 'eala' 3D Surround Function
- 'eala BASS' Dynamic Bass Boost Function
- 5band-PEQ
- Automatic Gain Control
- Tone Control
- 3.1-Channel Outputs including Center speaker and Subwoofer

■ Digital Signal Processor Specification

- 24bit Fixed-point Digital Signal Processing
- Maximum System Clock Frequency   : 38MHz
- Digital Audio Interface   : 2 Input ports / 2 Output ports
- Master / Slave Mode
- Master Mode MCK   : 1/2 fclk, 1/3 fclk
        ex. MCK = 384Fs(1/2) or MCK = 256Fs(1/3) at fclk=768Fs
- Two kinds of micro computer interface
    - I^2C bus (standard-mode/100kbps)
    - Serial interface (4 lines: clock, enable, input data, output data)
- Power Supply   : 2.5V (3.3V Input tolerant)
- Package   : QFP32-R1

    The detail hardware specification of the NJU26105 is described in the ' NJU26100 Series Hardware Data Sheet'.

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NJU26105

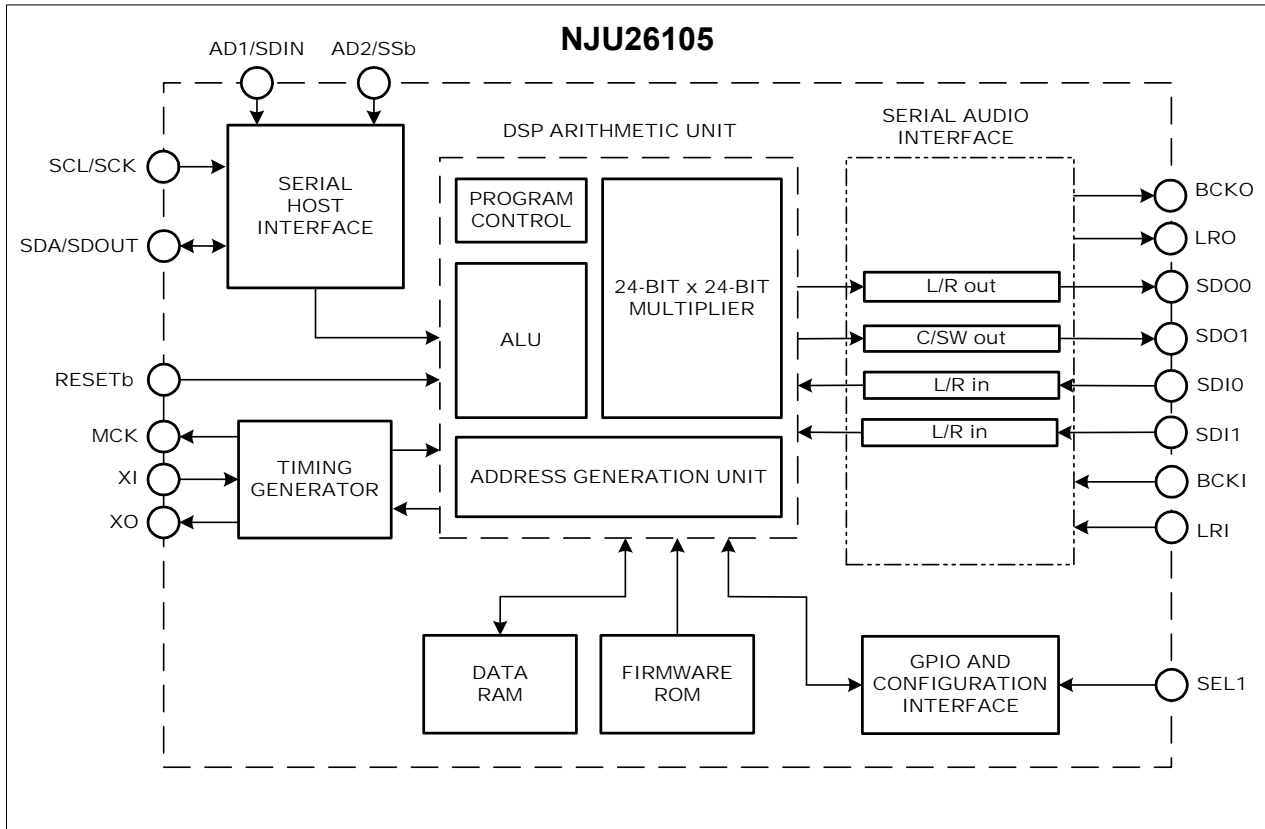## ■ Function Block Diagram

Fig. 1   NJU26105 Block Diagram
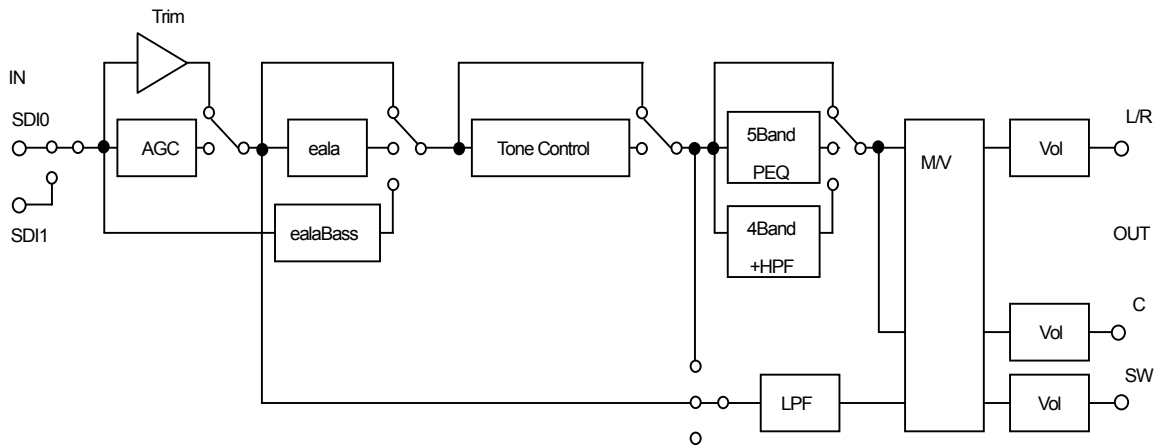
■ DSP Block Diagram

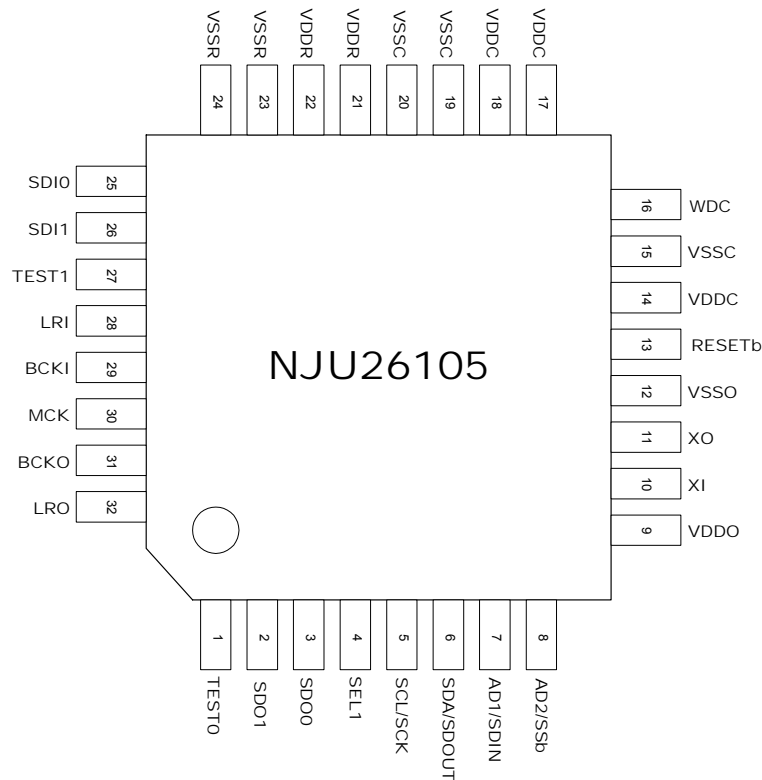**Fig. 2   NJU26105 Function Diagram**

■ Pin Configuration

Fig. 3   NJU26105 Pin Configuration

■ Pin Description

Table 1   Pin Description

No.	Symbol	I/O	Description	No.	Symbol	I/O	Description
1	TEST0	O	Open	17	VDDC	--	Core Power Supply +2.5V
2	SDO1	O	Audio Data Output 1 C/SW	18	VDDC	--	Core Power Supply +2.5V
3	SDO0	O	Audio Data Output 0 L/R	19	VSSC	--	Core GND
4	SEL1	I ^{*2}	Select I^{2}C or Serial bus	20	VSSC	--	Core GND
5	SCL/SCK	I	I^{2}C Clock / Serial Clock	21	VDDR	--	I/O Power Supply +2.5V
6	SDA/SDOUT	I/O	I^{2}C I/O / Serial Output	22	VDDR	--	I/O Power Supply +2.5V
7	AD1/SDIN	I	I^{2}C Address / Serial Input	23	VSSR	--	I/O GND
8	AD2/SSb	I	I^{2}C Address / Serial Enable	24	VSSR	--	I/O GND
9	VDDO	--	OSC Power Supply +2.5V	25	SDI0	I	Audio Data Input 0 L/R
10	XI	I	X'tal Clock Input	26	SDI1	I	Audio Data Input 1 L/R
11	XO	O	OSC Output	27	TEST1	I	Connect to GND
12	VSSO	--	OSC GND	28	LRI	I	LR Clock Input
13	RESETb	I	RESET (active Low)	29	BCKI	I	Bit Clock Input
14	VDDC	--	Core Power Supply +2.5V	30	MCK	O	Master Clock Output
15	VSSC	--	Core GND	31	BCKO	O	Bit Clock Output
16	WDC	O ^{*2}	Clock for Watch Dog Timer	32	LRO	O	LR Clock Output

*1 I : Input, O : Output, I/O : Bi-directional

*2 SEL1 : Input, WDC : Output

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■ Audio Interface

The NJU26105 audio interface provides industry serial data formats of I^2S, MSB-first Left-justified or MSB-first Right-justified. The NJU26105 audio interface provides two data inputs, SDI0 and SDI1, and two data outputs, SDO0 and SDO1, as shown in table 2 and 3. The input serial data is selected by the firmware command.

Table 2   Serial Audio Input Pin

Pin No.	Symbol	Description
25	SDI0	Audio Data Input 0 L / R
26	SDI1	Audio Data Input 1 L / R

Table 3   Serial Audio Output Pin

Pin No.	Symbol	Description
3	SDO0	Audio Data Output 0 L / R
2	SDO1	Audio Data Output 1 C/SW

■ Host Interface

The NJU26105 can be controlled via Serial Host Interface (SHI) using either of two serial bus formats : I^2C bus or 4-Wire serial bus. Data transfers are in 8 bits packets (1 byte) when using either format. The SHI operates only in a SLAVE fashion. A host controller connected to the interface always drives the clock (SCL / SCK) line and initiates data transfers, regardless of the chosen communication protocol.

The detail I^2C bus and 4-Wire Serial bus information are described in the 'NJU26100 Series Hardware Data Sheet'.

■ I^{2}C address

AD1 and AD2 pins are used to configure the seven-bit SLAVE address of the serial host interface. These pins offer additional flexibility to SLAVE address. 4 addresses could be chosen by AD1 and AD2-pin. The AD1 and AD2-pin addresses are decided by the connections of AD1 and AD2-pin. The AD1 and AD2 addresses should be the same level as AD1 and AD2-pin connections.

Table 4   I^{2}C Bus SLAVE Address

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0	0	1	1	1	AD2*	AD1*	R/W

*AD1 or AD2 address is 0 when AD1 or AD2-pin is 'Low'.
*AD1 or AD2 address is 1 when AD1 or AD2-pin is 'High'.

The detail I^{2}C bus timing of the NJU26105 is described in the ' NJU26100 Series Hardware Data Sheet'.

■ 4-Wire Serial Interface

The serial host interface can be configured for 4-Wire Serial bus communication by setting GPIO0 pin (*SEL1 pin)='High' during the Reset initialization sequence. SHI bus communication is full-duplex; a write byte is shifted into the SDIN pin at the same time that a read byte is shifted out of the SDOUT pin. Data transfers are MSB first and are enabled by setting the Slave Select pin Low (SSb = 0). Data is clocked into SDIN on rising transitions of SCK. Data is latched at SDOUT on falling transitions of SCK except for the first byte (MSB) which is latched on the falling transitions of SSb. SDOUT is Hi-Z in case of SSb = 'High'. SDOUT is CMOS output in case of SSb = 'Low'. SDOUT needs a pull-up resistor when SDOUT is Hi-Z.

The detail 4-Wire Serial bus timing of the NJU26105 is described in the ' NJU26100 Series Hardware Data Sheet'.

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■ Firmware Command Table

Host processor can control the NJU26105 via I^{2}C bus or 4-Wire serial bus interface. The following table summarizes the available user commands.

Table 5   NJU26105 Command

No.	Command	Command Description
1	Start Command	A command receivable state
2	System State	Serial Mode, Data Width, MCK, BCK, Master / Slave
3	Firmware mode select	3D, PEQ, AGC, Tone Control, SW mode
4	Fs Select / Input Select	32, 44.1, 48kHz, SDI0, SDI1
5	Master Volume	0dB to -96dB, -inf
6	Master Volume Boost	Boost : 0, 6, 12, 18, 24dB
7	Master Volume Smooth Control	Smooth Control : 13, 26, 53, 106ms
8	Channel Balance	0dB to -30dB, -inf, L/R
9	Output Channel Trim L/R	0dB to -96dB, -inf, L/R
10	Output Channel Trim C/SW	0dB to -96dB, -inf, C/SW
11	AGC Threshold Level	-6dBFS to -40dBFS
12	AGC Noise Compressor Threshold Level	-50 dBFS to -96dBFS, -inf
13	AGC Attack Time / Release Time	AGC Attack Time : 0.1, 0.2, 0.5, 1, 2, 5 [sec] AGC Release Time : 1, 2, 5, 10, 20, 50 [msec]
14	AGC Ratio / Boost	AGC Boost : 0, 6, 12, 18, 24dB AGC Ratio : 20:1, 8:1, 4:1, 2:1, -inf
15	AGC Output Trim	0dB to -31dB
16	AGC BYPASS Trim	0dB to -31dB
17	eala Surround Gain	0dB to +12dB
18	eala Bass Bass fo	40Hz to 315Hz
19	eala Bass Bass volume	-12dB to +12dB
20	eala Bass Treble fo	8kHz, 9kHz, 10kHz, 11kHz
21	eala Bass Treble gain	0dB to +6dB
22	eala Bass Output Trim	0dB to -31dB
23	eala Bass Attack Time / Release Time	AGC Attack Time : 0.1, 0.2, 0.5, 1, 2, 5 [sec] AGC Release Time : 1, 2, 5, 10, 20, 50 [msec]
24	Tone Control Bass/Treble Gain	-12dB to +12dB
25	EQ band1 mode	PEQ, HPF
26	PEQ1 to 5 / HPF fo	20Hz to 20kHz(20point/decade)
27	PEQ1 to 5 Q	0.33, 0.43, 0.56, 0.75, 1, 1.2, 1.5, 1.8, 2.2, 2.7, 3.3, 3.9, 4.7, 5.6, 6.8, 8.2
28	PEQ1 to 5 Gain	-12dB to +12dB
29	SW fc	40Hz to 315Hz
30	Version No. Request	Firmware Version No. Request

No.	Command	Command Description
31	Status Read	Status inside DSP is outputted.
32	AGC Input Level Request	AGC Input Level is outputted.
33	AGC Gain Reduction Level Request	AGC Gain Reduction Level is outputted.
34	No Operation	NOP command

■ License Information

Purchase of I^{2}C components of New Japan Radio Co., Ltd or one of sublicensed Associated Companies conveys a license under the Philips I^{2}C Patent Rights to use these components in an I^{2}C system, provided that the system conforms to the I^{2}C Standard specification as defined by Philips.

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